REMARKS/ARGUMENTS

Claims 2, 4, 10-13 were presented for examination and all were rejected in an Office Action dated May 12, 2005. Applicant herein responds to the rejected claims and adds a new claim 14. Applicant respectfully requests reconsideration in light of the below remarks and allowance of pending claims 2, 4, 10-14.

Claim 12

Claim 12 was rejected under 35 USC 102(e) as being anticipated by Frey (US Patent No. 6,430,720) and under 35 USC 102(b) as being anticipated by Attaway (US Patent No. 5,872,793). Frey discloses a memory that stores pre-computed test vectors but fails to recite any description of "a programmable test vector generator." As stated in the detailed description, "the test vectors are generated in real time" (page 2, line 12) as compared to Frey in which pre-computed test vectors are stored within a memory device.

Attaway discloses test vectors generated within a BIST but fails to disclose "an external tester" to generate test vectors for the logic circuitry. Accordingly, Applicant respectfully submits that neither Frey nor Attaway disclose each element within claim 12 and that the rejections under 35 USC 102 be withdrawn.

Claims 13 and 14

Claim 13 was rejected under 35 USC 103(a) as being unpatentable in light of Frey (US Patent No. 6,430,720) and Barry (US Patent No. 5,825,785). Applicant has rewritten claim 13 independent form.

In his rejection, the Examiner argues that the combination of Frey and Barry would be appropriate because "the combination would provide the procedure disclosed in Frey with a technique whereby 'test vector application to inputs of said embedded macro circuit causes said embedded macro circuit to generate a response on the parallel outputs for serially shifting said response from said scan register into a

serial input shift register such that each subsequent response is serially compressed..."" (quoting Barry col. 8 line 45 et. seq.) The Applicant respectfully submits that a motivation to combine the two references has not been established by the Examiner.

"Obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either explicitly or implicitly in the references themselves or in the knowledge generally available to one of ordinary skill in the art." (MPEP §2143.01) Applicant submits that there is not any disclosure in Frey to suggest providing "a compact representation of said test results" to an external tester. Barry does not teach nor suggest that any test results are provided to an external source; rather, the purpose of Barry "is to provide an improved built-in self test design and method for verification of *embedded devices or macros*." (Barry col. 2, lines 23-25) Furthermore, the quoted text (Barry col. 8 line 45 et. seq.) that the Examiner uses as motivation to combine the references is describing a testing device for memory ICs, not logic circuitry as disclosed in claim 13. Accordingly, the Applicant respectfully argues that the combination of Frey and Barry lacks support, is improper and constitutes impermissible hindsight.

Claim 14 describes providing the external tester test vectors to enable fault localization on the logic circuitry. Applicant submits that this claim is allowable in view of the cited references.

Claim 11

Claim 11 was rejected under 35 USC 103(a) as being unpatentable in light of Frey (US Patent No. 6,430,720) and Barry (US Patent No. 5,825,785). Applicant respectfully disagrees with the Examiner and requests reconsideration in view of the comments below.

Claim 11 recites means for "producing a compact representation" of a test result and outputting the "compact representation to the external tester." For the reasons described above, the Applicant asserts that the combination of Frey and Barry is improper in the rejection and that this claim is allowable in light of these two references.

Claims 2, 4, 5, and 10

Claims 10 was rejected under 35 USC 103(a) as being unpatentable in light of Frey and Barry. The Examiner argues that the teachings in Frey suggest "By replacing the large test memory with a test pattern generator, one of ordinary skill in the art would save IC space and cost by not having to implement the test vectors in large memories." However, as described above, Frey fails to disclose a programmable test vector generator because Frey, as the Examiner admits, discloses the use of pre-generated test vectors stored within memory. Frey does not suggest the use of such a programmable test vector, and in fact, teaches the use of storing test vectors in order to synchronize the test pattern to a clock. Furthermore, the Applicant respectfully asserts that the combination of Frey and Barry is improper for reasons discussed above. Accordingly, the Applicant requests that the rejection be withdrawn and that claim 10 be allowed in light of the above-described reasons.

Claim 4 was rejected under 35 USC 103(a) as being unpatentable over Frey in light of Barry and Attaway. As described above, Frey fails to disclose a programmable test vector generator, and accordingly, each element of claim 4 was not described in the combined references. Furthermore, the Applicant respectfully argues that the combination of Frey, Barry and Attaway is even more problematic than the combination of Frey and Barry discussed-above. In particular, motivation for adding Attaway to the Frey/Barry combination is not present as Attaway teaches testing methods for memory integrated circuits not logic circuitry. The statement that the combination is proper because "result storage requirements are optimized" fails to provide any support or motivation within any of the three documents. Accordingly, the Applicant respectfully asserts that the rejection be withdrawn and that claim 4 be allowed in light of the above-described reasons.

Claim 5 was rejected under 35 USC 103(a) as being unpatentable over Frey in light of Barry, Attaway, and Derwent (Abstract ACC-NO 1988-141950). For the reasons discussed above, the Applicant respectfully argues that the combined references fail to disclose a programmable test vector generator and that the combination of the references is improper because the documents fail to suggest a

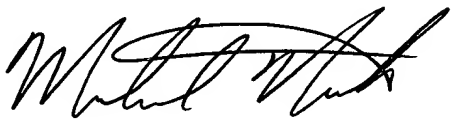
reason or motivation for the combination. Accordingly, the Applicant respectfully asserts that the rejection be withdrawn and that claim 5 be allowed.

Claim 2 was rejected under 35 USC 103(a) as being unpatentable over Frey in light of Barry. The Applicant reiterates his argument that the combined references fail to disclose a programmable test vector generator and that the combination of the references is improper because the documents fail to suggest a reason or motivation for the combination.

CONCLUSION

In view of the above arguments and amendments, Applicant believes that all pending claims are allowable and respectfully request a Notice of Allowance for this application from the Examiner.

Respectfully submitted,
NORTH WEBER & BAUGH



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